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WLAN System, HW, and RFIC Architecture for the Intel® PRO/Wireless 3945ABG Network Connection

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WLAN System, HW, and RFIC Architecture for the Intel® PRO/Wireless 3945ABG Network Connection

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ABSTRACT

The corporate challenge of being "one generation ahead" has prompted us to find new ways to improve our time to market, size, and cost of our WLAN products. By identifying the key issues which challenged us in our previous-generation products and by shifting our design effort to a platform-level optimization, we moved to a top-down approach in our Si and hardware architecture design flow. By taking the product-level requirements down to the last component on the board using this new methodology, we enabled smoother and cleaner platform integrations, as well as smaller and cheaper solutions. This paper summarizes the different architectural and functional changes in our products, from the system level down to the board/Si level. In addition, we discuss some of the design issues to ensure robust and reliable RF designs in our radio chips. The Intel® PRO/Wireless 3945ABG Network Connection, which is a part of Intel® Centrino® Duo mobile technology, is the first Intel® WLAN product to be conceived in this way.

INTRODUCTION

The corporate challenge of being "one generation ahead" in our WLAN product line has challenged us to improve our time to market, product size, and cost. To achieve these goals, we take a top-down approach to our Si and hardware designs in order to optimize platform development. This top-down approach led us to consider the product-level requirements down to the last component on the board, which not only enabled smoother platform integration, but also cheaper products. In this paper, we describe the overall approach used in the development of the Intel PRO/Wireless 3945ABG Network Connection, which is part of Intel Centrino Duo mobile technology, and is the first Intel WLAN product to be conceived using this new top-down approach.

The Intel PRO/Wireless 3945ABG Network Connection conforms to the IEEE 802.11a/b/g/d/e/h/i standards and supports data rates from 1 Mbps up to 54 Mbps. It is capable of transmitting output powers up to 18dBm. It operates in the 2.400-2.484 GHz and 5.17-5.85 GHz frequency ranges and supports a Wake on Wireless LAN (WoWLAN) feature.

In this paper we summarize the different architectural/functional design approaches and tradeoffs taken from the system level down to the board and transistor level on Si. First, we summarize the system, board, RFIC, and front-end module architectures. Next, we discuss the design considerations and tradeoffs for each of the architectures. Finally, we summarize the high-volume testing challenges that had to be overcome to enable a reduction in production test time by a factor of 3, from 104 to 32 seconds per card for the wireless platform. The salient features and successes of this overall methodology can be seen in a reduction in the platform integration cycle time from 6 to 4 quarters, a "world class" wireless solution yield improvement through self calibration schemes to better than 98.5%, a modularity approach with built-in reliability checks to the RFIC design flow, migration to a smaller form factor (FF) platform solution (single-sided Mini card) with the lowest part count for this FF class, and a lower product cost achieved through customized board elements and vendor multisourcing.

ARCHITECTURE

System Architecture

The block diagram of the Intel PRO/Wireless 3945ABG Network Connection is shown in Figure 1. The system is composed of two chips, fully designed by Intel, and other third-party board components. One chip contains all the digital and mixed signal components including analog to digital converter (ADC) and digital to analog converter (DAC) while the other contains the RF sections. The media access control/baseband (MAC/BB) chip consists of the host interface, MAC processor, BB subsystem (OFDM and CCK modem), and the ADC/DAC. The RFIC chip consists of the synthesizer and full transmit/receive (TX/RX) chains, from BB to RF.

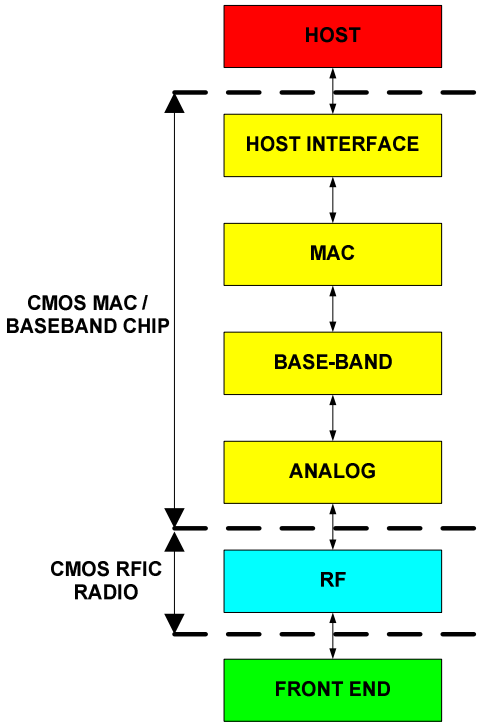

Figure 1: System block diagram of the Intel PRO/Wireless 3945ABG Network Connection

Board Architecture

The board architecture shown in Figure 2 was based on the silicon partitioning and so we had four main sections:

1. The MAC/BB with an associated EEPROM (non-volatile memory) used to store all board-specific information (MAC address, calibration data, regulatory skew information, etc.). The MAC/BB is also the only section that directly interfaces with the platform through the PCI Express* Mini Card interface.
2. The RFIC with an associated Xtal device used to generate all on-board frequencies and clock signals.
3. A bias network to enable bias selection, voltage regulation, and power management needed by the system.
4. An RF Front End (FE) section comprises antenna and transmit/receive switches, power amplifiers, low-noise amplifiers, and filtering devices.

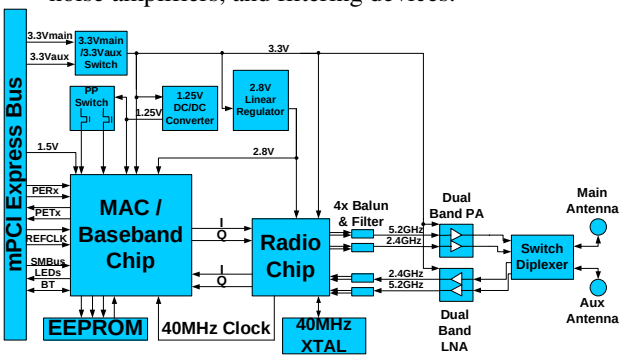

Figure 2: Block diagram of the board architecture

RFIC Architecture

The Si radio chip was designed using 0.18 um CMOS. The floorplan of the radio was designed together with the front end module (FEM) and package to minimize the spatial mismatch between the chip I/Os with the elements on the board. The architecture of the radio is shown in Figure 3 and is subdivided into six blocks: synthesizer, logic, RX BB, RX RF, TX BB, and TX/RF blocks. The logic section receives instructions from the MAC chip to set the system state. The instructions are then processed and output to the different blocks. The synthesizer is driven by an external clock. The loop basically can switch between two states to provide the LO signal for the low-band 802.11b/g (2.4-2.5 GHz) and the high-band 802.11a (4.9-5.95 GHz) up/down converters in the TX/RX chains. The dual-band RX chain consists of two separate RX architectures at the high- and low-bands, respectively. Note that the noise figure of the off-chip low noise amplifier (LNA) on board fixes the overall RX chain noise figure. A saturation detector at the input to the down converter is used to detect the power level in the receiver and if the power is too high, the attenuator at the input of the RX chain is triggered. The I/Q (in-phase and quadrature) signals from the down converter then pass into the BB section consisting of automatic gain control and active filters. The active filters will provide the out-of-band signal rejection depending on the system mode (CCK versus OFDM, etc.). The I/Q outputs from the BB section are passed off-chip via the board to the MAC chip.

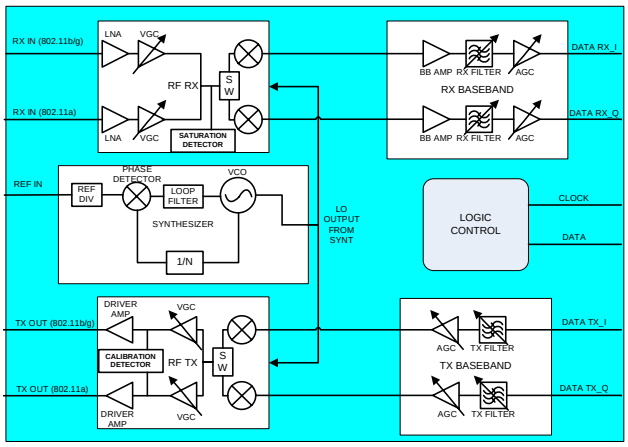

Figure 3: Block diagram of the RFIC architecture

On the TX side, the I/Q data signals from the MAC chip enter the radio chip via the TX BB section where they are filtered depending on the Wi-Fi standard needed, amplified via the digital gain control amplifier, and then upconverted to RF. The RF TX section consists of a high pass filter to reduce unwanted spurs at the lower bands followed by gain controlled amplifiers and a driver amplifier to the off-chip power amplifier (PA). A calibration detector at the input of the driver stage is used for calibrating the I/Q imbalance in the system.

Front End (FE) Architecture

The FE architecture shown in Figure 4 was basically defined at the system level which then drove the actual FE component content and requirements. The architecture chosen was a TX/RX architecture where the like TX and RX sections were all bundled together. This architecture also bundled similar technologies together according to the subgroups. For example, the PAs are of the same pseudomorphic high electron mobility transistor (PHEMT) GaAs technology, and the LNAs are of the same heterojunction bipolar transistor (HBT) GaAs technology. The filter passives are of a third technology and typically integrated in low temperature cofired ceramic (LTCC) technology. Therefore, the FE was subdivided into four category types: a) dual PA, b) dual LNA, c) switch-diplexer module, and d) balun filters. This "bundling" scheme ultimately created an industry trend of dual PA and LNA components appearing on the market place.

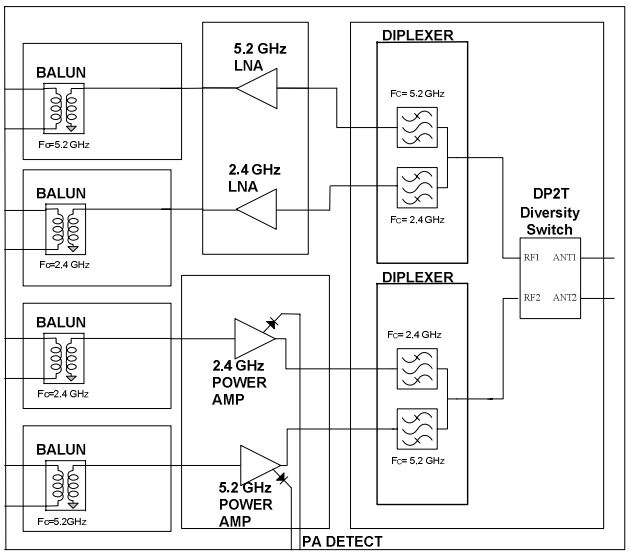

Figure 4: Front End architecture

DESIGN CONSIDERATIONS AND TRADEOFFS

System Tradeoffs

Once the marketing requirements for the product were released, the Intel PRO/Wireless 3945ABG Network Connection was partitioned down to the last detail. The architecture team developed the features and requirements of the different chips (MAC-BB, RF, and FE modules), while the system engineering team ensured that the different flows and features between the chips, board, and other components were synchronized and optimized. The two teams worked iteratively with each other such that the system team provided feedback on its findings/requirements to the architecture team in order for the architecture team to implement them in the chip design.

Another key point was to integrate the knowledge gained and avoid the pitfalls of previous projects. Since many of the system engineers led or were part of the integration of previous products, their input as to how to improve our product development approach was invaluable. Closing this loop was the only way to ensure that the next product integration cycle would be seamless and smooth.

There is a big difference between the design of the WLAN system of a few cards versus that of millions in production. All the manufacturing issues were taken into consideration from the start in order to guarantee a very robust and stable system. One important change was to utilize self-calibrations in order to compensate for component-to-component variance. From the early stages of the project, we obtained models about these variances and designed on-chip calibrations to compensate for them.

These calibrations guaranteed that millions of boards in production will behave with minimal performance deviations between them in accordance with the product specification. Ultimately, this contributed to very high yields in production. For example, in every WLAN system, the TX power needs to be calibrated. On the one hand, we want to transmit as much power as possible, but on the other hand, we cannot surpass regulatory limits. In previous projects, we used open loop calibration, but in the Intel PRO/Wireless 3945ABG Network Connection, we implemented a closed-loop TX power calibration shown schematically in Figure 5. It is important to note here that these self calibrations illustrate the kinds of things that can be done when designing the system from top to bottom. Other self calibration schemes were used to compensate for RF/analog parameter variances (I/Q imbalance, DC offset, gain, etc.), but for simplicity and cost reasons, these are compensated for in the digital domain.

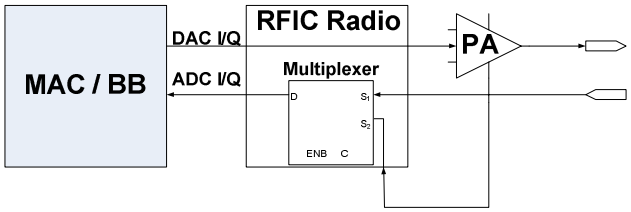

Figure 5: Closed-loop TX power calibration scheme

RFIC Design Considerations

The Radio Frequency Integrated Circuit (RFIC) designs used in the radio chip for the Intel Centrino Duo mobile technology are basically a concatenation of different functional blocks (amplifier, mixer, etc.) to form transmit or receive subsystems. The optimal (and real-estate savings) method for designing these subsystems would be to provide an impedance match between each of the blocks. Essentially the design then becomes one complete, standalone subsystem block. The other extreme is to design modular subsystem blocks, matching them all to the same impedance level and concatenating the blocks. Although not necessarily optimal in terms of real estate and power consumption, the system design is robust. Basic circuit theory dictates that if a design has a high impedance between two cascaded circuit blocks, the voltage is transferred between them. This is more useful for analog circuits and mixers. On the other hand, if the impedance is low, current is predominantly transferred between the two blocks. Microwave engineering usually looks at power transfer using impedance levels at 50 ohm, with power gain and match (return loss) as the primary metrics. If each of the blocks is matched to 50 ohm (or 100 ohm for differential circuits), these modular blocks can usually be seamlessly concatenated, without any significant increase in loss over the bandwidth in question. Moreover, these blocks can better withstand any changes in process variations or model inaccuracies; hence, they become predictable both in design and performance.

The prime consideration in our silicon RF CMOS designs was how to succeed in getting the product out to the market on time, reliably. In order to reduce design risk for this product, we leveraged the element of predictability described above. Thus, our approach here was to modularize all of the radio chip RF sub-blocks by designing each block independently to 50 ohm (or a 100 ohm differential) and to concatenate them. Analog designers typically utilize parasitic extraction to model coupling, capacitive loading, and fanout between the myriad of signal interconnects between circuit blocks. With RF designs at frequencies as high as 6 GHz and the need to check for harmonic performance and circuit stability up to 20 GHz, this "analog" approach is not accurate enough at these frequencies to account for distributed effects and unwanted coupling. Thus, the entire RF portions of the circuit layout were simulated in an electromagnetic (E/M) simulator to account for these effects. The output from the E/M simulator is then brought back into the circuit simulator for further analyses capturing all the E/M effects in the design simulations for maximum accuracy. This approach is illustrated in Figure 6.

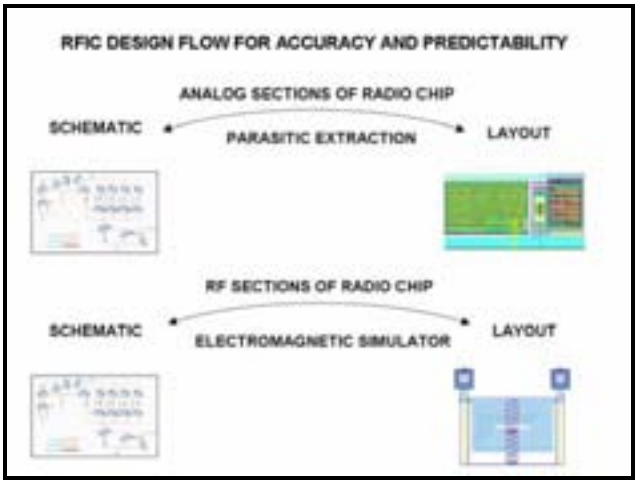

Figure 6: RFIC design flow for performance accuracy and predictability

Once the designed circuit blocks are concatenated into the RF RX/TX subsystems, which are then simulated, the circuit block and overall radio chip layout underwent reliability simulations such as aging, time dependent dielectric breakdown, IR drops in the power supply lines, and electromigration degradation checks in the inductors. For aging, the dominant aging effects of hot carrier injection in NMOS and PMOS, as well as negative bias temperature instability in PMOS transistors, were

considered. In the circuit simulations, the aged transistor models were then used to recompute the aged RF performance on the radio chip circuit blocks [1]. Electromigration effects were determined by parasitic extraction tools in looking at whether the inductor elements have enough metallization to carry the DC reliably.

Board Tradeoffs

The Intel PRO/Wireless 3945ABG Network Connection WLAN solution was required to fit on to a new FF, called Mini Card (PCI-SIG PCI Express Mini Card CEM), to be used on the Intel Centrino Duo mobile technology platform [2]. This new FF is about half the size of a Mini PCI card Type A used in the previous-generation WLAN solution called the Intel® PRO/Wireless 2915ABG Network Connection. An additional constraint was to have a single-sided solution, which meant that we had less than a quarter of the original board real estate available to implement the solution. This required us to rethink our board strategy and review our architecture. The new board architecture and strategy were driven by a number of key directives:

1. Keep it simple (simple and direct interfaces to optimize routing).
2. Optimize package selection and pinouts (to enable component butting).
3. Design for High-Volume Manufacturing (HVM) from the beginning.
4. Optimize for low-cost Printed Circuit Board (PCB) technology (minimum number of layers, through-hole vias, industry-standard design rules).
5. Optimize bias networks for simplest implementation (minimum number of power rails, unification of power rails, efficient power conversion schemes, minimum number of parts).
6. Outsource all components to multiple vendors to enable a significant cost reduction through competition between vendors.

Keeping the design as simplistic as possible is probably the main directive that drove the design. The intent was to design all of the components in such a way that their actual implementation on the board would be very much like the drawing of its block diagram. The interfaces between the different blocks/packages/silicon would need to coincide with each other to prevent unnecessary crossover routing on the board. All of the RF routing was limited to the top side only so as to minimize regulatory infringements (radiation, emissions) and enable easy certification by the various regulatory bodies. Keeping it simple also meant that we needed to drastically reduce the part count. The product requirement document clearly indicated that a single hardware (HW) skew would be supported, such that one HW build configuration made all of the logistics much simpler.

Another key directive was the optimum package selection for the silicon chipset where the pinouts between the MAC and RFIC chips were aligned to each other allowing for direct interconnect on the board. This approach enabled us to save significant board space.

The strategy of Design For Manufacturing (DFM) of HVM from the beginning of the design enabled us to identify potential limitations early in the program cycle. Once identified, the DFM infringements were dealt with in various manners. Some required a re-layout of specific sections on the product board. Some required the Manufacturing Engineering Group to re-examine outdated design rules for validity as the PCB fabrication and assembly technology matured over time. Some of the rules were modified quickly, and some rules required more extensive investigation including experimental assembly runs to check the validity of the rule intended to maintain low DPM requirements. By implementing the DFM/HVM rules from the beginning of the design, the 3945ABG was mass produced with very high production yields greater than 98.5%. This significantly reduced the product cost.

Product cost is always the driving factor in our development solutions. The PCB was found to be a significant cost percentage of the Bill of Material (BOM). As such we researched the PCB parameters that are "cost adders." We identified that the PCB material is a cost adder, whereas FR4-based materials are the cheapest. The type/class is another cost adder, whereas Through Hole Via (THV) technology would yield the lowest cost PCB. The number of layers and the exposed pad plating were also cost adders. Multiple vendors were requested to provide their technological capabilities with respect to the proposed PCB stackup and material. Once we found the lowest common denominator tolerances of multiple vendors, we specified the PCB so all vendors could comply with their existing capabilities and thus enabled cost reduction through competition and outsourcing to multiple vendors. The net result is that the Intel PRO/Wireless 3945ABG Network Connection incorporates a 4-layer FR4 with THV to achieve the lowest possible cost PCB solution that met our needs.

Our previous-generation WLAN board design had nine power rails, which was a tremendous cost adder because of the increased board real estate. The new FF Mini Card with the limited board real estate dictated that we re-examine the bias network strategy and drastically simplify it. The only way this could be done on the Intel PRO/Wireless 3945ABG Network Connection and the Si chipsets was to unify the bias voltages or generate them directly on die without adding any more circuitry to the board. Since the MAC and RFIC chips are fabricated on different CMOS processes, it was difficult to find a perfect unification of the power rails between the chips. A

compromise was reached that enabled the unification of the Analog/RF voltage with a single voltage to be used by both chips. In this way, the 2.8 V would be generated on the board by means of a linear regulator. The digital core voltage of the RFIC needs to be 1.8 V due to process requirements, but since it is a low current consumption rail, it was generated and regulated on-die. On the other hand, the core voltage of the MAC/BB chip (1.25 V) is one of the larger power consumers and therefore it was generated on-board by means of a DC/DC converter in order to save power. Another specific voltage is required for another dedicated circuit in the RFIC. The 2.5 V on-die regulator was dedicated to supply the voltage to the internal VCO, which requires a very clean and stable voltage supply to meet the RF performance of the system. Because our system is intended for very low-power consumption platforms, additional means were used to further reduce the leakage currents in idle and disabled modes of operation. The use of power plane separation switches enabled us to shut off the bias supply to the two largest digital circuit blocks (the MAC and PHY) to eliminate leakage currents. The final component in our bias network is a bias selection switch used to select between the 3.3 V main and the 3.3 V auxiliary power rails from the platform to enable wake-on WLAN (WoWLAN) modes during system (Sx) states. The 1.5 V power rail from the platform is dedicated to the PCI Express engine and connects directly to the MAC chip.

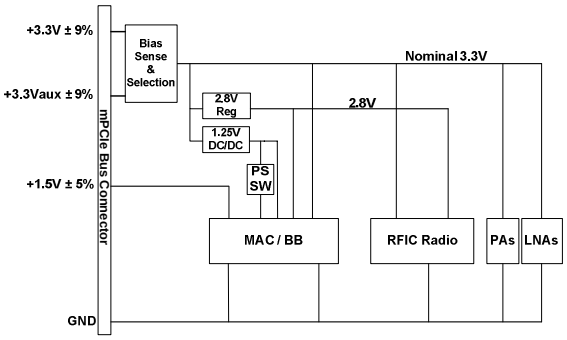

Figure 7: Bias network on the Intel PRO/Wireless 3945ABG Network Connection card

The other key components, such as the FE components, were specified by Intel as per our system needs. Specification documents were distributed among the potential vendors. Having multiple vendors providing us with the same "black box" component enabled us to outsource the product to multiple vendors to ensure a continuous supply base and a cost reduction through competition between the vendors. This strategy was initially targeted for the more expensive RF components (e.g., the power amplifiers, the low noise amplifiers, the switches and the passive filtering devices), but we expanded this strategy to cover other key components such as the EEPROM, the Xtal, and the bias network components. This multi-sourcing scheme not only enabled lower overall cost (through vendor competition), but also helped the design team to better understand the expected material variation resulting in a more robust "HVM-friendly" design that has built-in margins to compensate for expected material variations. Therefore, the design is less susceptible to yield fluctuations.

One of the key unknowns with respect to the new Mini Card FF was PCI Express noise leakage into the receiver and how this would affect product performance. The first generation PCI Express standard high-speed signals generate energy as high as our 2.4-2.5 GHz frequency range of operation. There was concern that leakage of the PCI Express signal from the Mini Card interface section may reach the RF/RX chain and interfere with reception and performance. A series of investigations were done to examine what critical items in the design needed to be done to minimize this leakage. This study included electromagnetic simulations of the package and bond wire scheme. After having done this investigation, the silicon design of the PCI Express engine needed to become a very compact and bias independent section of the die. This also affected the pinout, and it required that the PCI Express interfaces in the silicon be as close as possible to the Mini Card interface connection including a ground pin ring that encompassed the active pins to shield the PCI Express pins from the other sections of the package. A unified ground plane scheme in the PCB was used, which yielded the best isolation behavior from one end of the board to the other. The shielding scheme was limited to the radio section only to further reject any stray leakage which could leak into our sensitive receiver.

Other noise sources needed to be taken into account, such as voltage bounce and current surges associated with transitions from one state to another. These noises could adversely affect the performance of the product because they disrupt key parameters like the frequency stability of the local oscillator used for all of the up and down frequency conversions. Special care needed to be taken in the PCB layout to ensure proper ground return paths for key components, such as the power amplifiers. This was done by strategically placing decoupling capacitors in the entire circuit and sequencing the transition events (instead of instantaneous transitions) so as to reduce their effect on the key frequency sources in the system.

FEM Tradeoffs

The Mini Card FF drove us to re-examine how to save space on the board. One of the largest consumers of board space in the Intel PRO/Wireless 2915ABG Network Connection product generation was the RF FE section. Therefore, it became apparent that if the FE section did not shrink drastically, we would not be able to fit it into a single sided Mini Card FF. The sheer number of

components dictated that some sort of integration was required. The question was how much could be integrated without jeopardizing the program schedule or reliability. Going from a discrete solution to a fully integrated solution with multi-sourcing was too high a risk for the program. Therefore, we chose to implement a block-level integration scheme.

We also realized that going to this block-level integration would require defining custom parts that suited our system needs. When looking at the FE architecture, it became obvious that by bundling the technologies together, we also attained the best integration as well. For example, taking the two PAs (one for each band) and integrating them on the same GaAs die, along with their respective bias networks, into a single package device would ultimately yield the smallest solution. For example, the PA circuit alone, which was over 20 components in the Intel PRO/Wireless 2915ABG Network Connection generation, was shrunk down to five components (one integrated Dual Band PA and four decoupling caps) in the Intel PRO/Wireless 3945ABG Network Connection solution by the use of building blocks.

The same approach was also used to shrink other sections of the FE such as the dual LNA device, the switch-diplexer module, and the two balun filter devices. The integration of these components in this manner enabled us to implement a cheaper, single-sided solution for our Intel PRO/Wireless 3945ABG Network Connection WLAN product. The net effect of this FE module shrinkage is outlined in red in Figure 8, going from the FE of the previous generation (Intel PRO/Wireless 2915ABG Network Connection) to the current Intel PRO/Wireless 3945ABG Network Connection product.

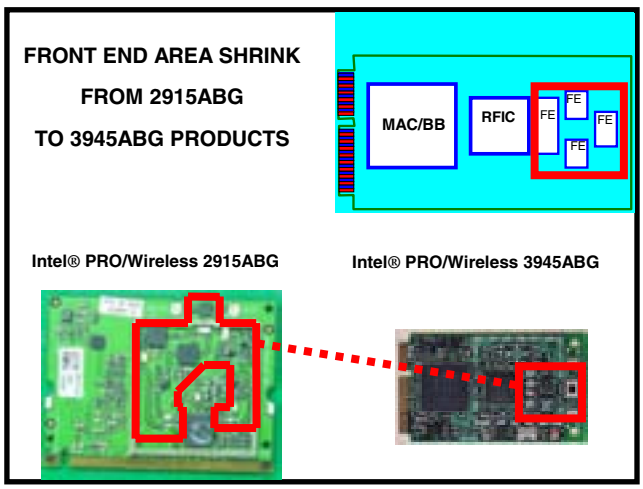

Figure 8: Front End module area compression from 2915ABG to 3945ABG

The main performance tradeoff between the various FE components was the out-of-band behavior. It was obvious that if we required one component to provide the entire out of band rejection needed for the system performance, it would make that particular component either very expensive, very large, or both. Therefore, when considering the RF line-up definition for the in-band performance, we also needed to distribute these out-of-band requirements between the three basic sections (balun filter, the active device, and the diplexer). Thus, we were able to simplify the requirements for each of the sections while achieving the overall system requirement. In some specialized cases, more weight needed to be placed on one section over another to compensate for known deficiencies or to maximize performance. For example, the diplexer rejection at frequencies below 2 GHz was stricter to prevent the LNA from saturating due to cell phone activity near the notebook platform. On the other hand, second- and higher-order harmonic signals needed to be reduced out of the PA to meet regulatory certification requirements, a requirement on the diplexer out of the PAs.

MANUFACTURING TESTING

One of the main bottlenecks in reducing product cost and time to market was the need to significantly reduce production testing time. The new approach described here for the Intel PRO/Wireless 3945ABG Network Connection enabled a dramatic reduction in test time by a factor of 3 from 104 to 32 seconds per card at the functional testing stage as compared to the previous WLAN product (the Intel PRO/Wireless 2915ABG Network Connection).

The Wireless HVM process flow involves several stages (see Figure 9), each of which is capable of detecting specific failures.

Structural Test uses X-ray laminography technology, which provides a virtual 3D image "slice" that blurs out all but the selected plane of focus. These 3D cross-section images of solder joints are then evaluated.

Functional Test (FT) station is the first stage where the Intel PRO/Wireless 3945ABG Network Connection device is inserted into the PC. FT has several goals:

1. Check for HW failures of the system and sub-components.
2. Characterize the device's physical parameters that have an impact on transmit and receive path performance. Tests belonging to this category are called *calibration procedures.*

3. EEPROM programming: HW definitions and results of the calibration tests are stored in the device's EEPROM.

The next stage of the HVM flow is **Final Assembly**. This is the stage where the wireless device is packed and wrapped with a Label Paper sticker.

The **Final Tester** is used to verify the programming of the EEPROM, including the MAC address for the device, conduct performance tests on 802.11a/b/g radios, and an association test with an Access Point (AP). After the Final Test is performed, samples of passed units are tested in Ongoing Quality Monitoring (OQM).

The **OQM Station** runs the same tests as in the Final Tester, but on a defined percentage of the manufactured product. The main requirement of the whole HVM process is that at this station, the Defects Per Million (DPM) level will be below 500 DPM.

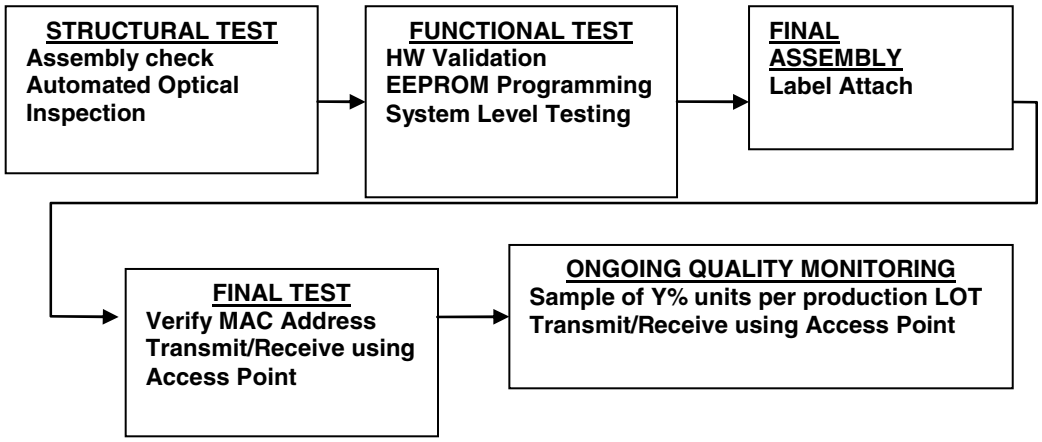

Figure 9: Intel PRO/Wireless 3945ABG Network Connection high-volume manufacturing process flow

Testing time and coverage are a major component of the manufacturing cost and quality of the wireless device, since they have a direct impact on the amount of equipment and testers that is used in the manufacturing line. In order to achieve so dramatic a reduction in testing time relative to our previous wireless products, several approaches were taken:

1. **Working over Product Network Driver (NDIS).** Our previous Intel® Wireless LAN products were tested using a specialized version of Validation Driver that was used to directly control the embedded software running on the product board. In the Intel PRO/Wireless 3945ABG Network Connection project, the role of the network driver was significantly enhanced and most of the features previously handled by the embedded software were moved to the driver level. Therefore, it made sense that the test and validation during FT should also be redone. This ultimately yielded a shorter test time of the product board. For example, the reset test flow through the Network Driver was optimized for speed. Over the Network Driver, it was 10 times faster than testing over an application layer-based test.
2. **Utilizing driver system flows**. Additional time savings were achieved by optimizing the time of validation flows. Using the Network Driver also made it possible to take advantage of real WLAN system-flows, such as online DC and TxIQ calibrations, and checking the embedded software image after reset. This enabled us to remove application-layer tests that did not contribute to the test suite coverage.
3. **Using** a **closed-loop TX power calibration algorithm.** By using this we dramatically reduced the amount of required measurement points in the FT tester, as compared to previous projects. This allowed the calibration to be performed in a much shorter time (by a factor of 2.5).
4. **Speeding up the equipment.** A special and dedicated effort was made to find the test equipment bottlenecks and to speed up the RF testing equipment used in the FT. Most of the time savings came from speeding up the Power Meter and Spectrum Analyzer equipment data acquisitions.

With regard to test coverage, in our previous projects of wireless HVM testing, there was always doubt as to how close the resemblance was between the driver and the FT software, since they represent two different flows. Using this new approach, this difference was eliminated because the FT was actually running using the same driver as the

product, giving us confidence in test quality and reliability. Overall test coverage was increased due to the fact that we were using the Product Network Driver in executing real-life system flows, such as online calibrations, real-time Tx/Rx flows, reset flow, and up-to-date PHY initialization routines. Having the network driver in manufacturing allowed logging of various system parameters across all manufactured boards, which helped us to monitor product health across builds.

Overall, by using the network driver for the Intel PRO/Wireless 3945ABG Network Connection FT made significant improvements to the Functional Tester Development Program in terms of time and coverage, and this technique will be used in our future Intel® Wi-Fi products.

CONCLUSION

This paper summarizes and reviews the work and design approach of many groups in the development of the Intel Centrino Duo mobile technology Intel PRO/Wireless 3945ABG Network Connection card for the Intel Centrino Duo mobile technology platform. The combination of taking a top-down approach to the system design, the application of self-calibration schemes, the modularity approach taken in the RFIC design, the use of custom board and FE elements to reduce part count, and the significant improvement of production testing time, has resulted in a reduction of platform integration from 6 to 4 quarters with product yields better than 98.5% with lower product cost and a smaller FF. The same approach is now being applied to our next-generation wireless products.

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REFERENCES

[1] M. Ruberto, T. Maimon, Y. Shemesh, A. Desormeaux, W. Zhang, C. Yeh, "Consideration of Age Degradation in the RF Performance of CMOS Radio Chips for High Volume Manufacturing," *IEEE RFIC Symposium*, Long Beach, CA, June 2005, pp. 549-552.

[2] "PCI Express Mini Card Electromechanical Specification," Revision 1.1; March 28, 2005, PCI-SIG.

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